--ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit includes a memory which has redundant lines for repair in both a column direction and a row direction. A test pattern generating section generates a specific test pattern for the memory. A comparing section reads an output from the memory to judge whether or not a fault cell exists in the memory and outputs a signal which shows existence or nonexistence of a faulty cell. The circuit includes a first data storage section, which operates in a first test mode for a test of the memory and a second test mode for a scan test, and a second data storage section which receives an output signal of the comparing section to store a state of presence or absence of a failure corresponding to the existence or nonexistence of the faulty cell. A repair judging section receives an input to the first data storage section and an output of retained contents in the first data storage section and judges that the memory is repairable. When the second data storage section is in a state where the failure exists, the first data storage section holds the data retained in the first data storage section.--